FIG. 1 (PRIOR ART)

PC
↓

| J → |

entering debug mode ~20

resume instruction 22

storing the
PC J in a register 24

performing debug process
without counting the steps ~26

leaving debug mode
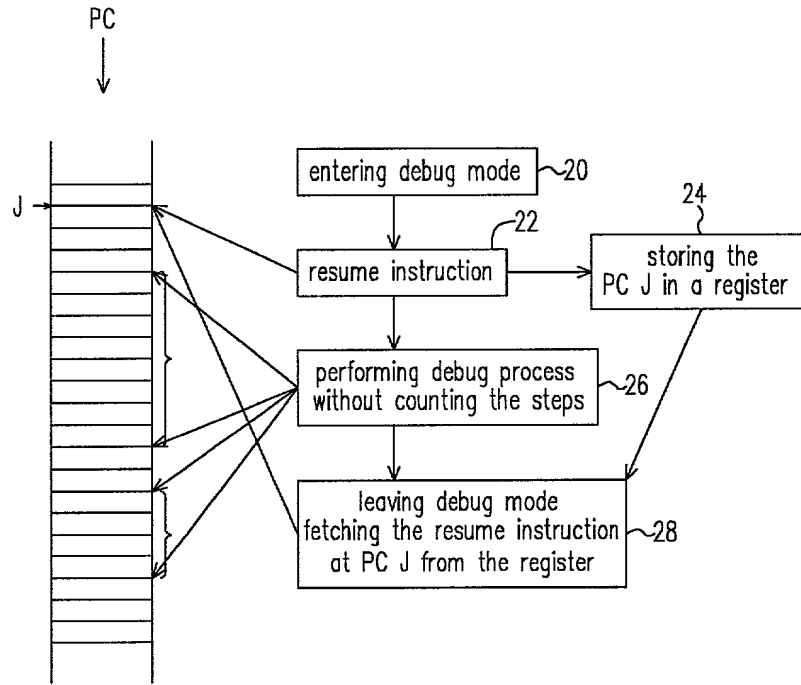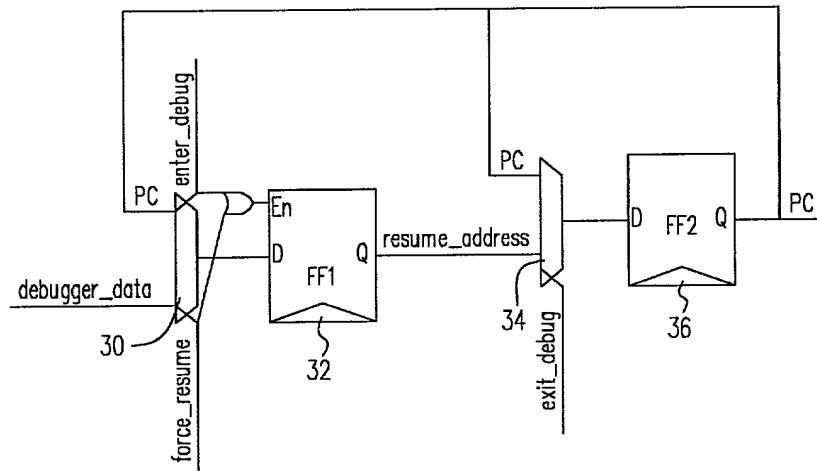fetching the resume instruction ~28
at PC J from the register

FIG. 2

when debug mode is entered, FF1 saves the PC.
when debug mode is exited, FF2 loades the saved PC.

FIG. 3